Global Standards for the Microelectronics Industry

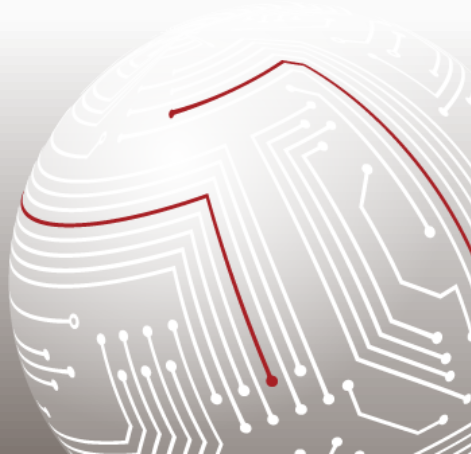
The CAMM2 Journey and Future Potential

- A short history of the CAMM2 journey since 2020
- Details on LPDDR5 CAMM2 and DDR5 CAMM2
- The future work and potential of CAMM2

CAMM2: Compression Attached Memory Module

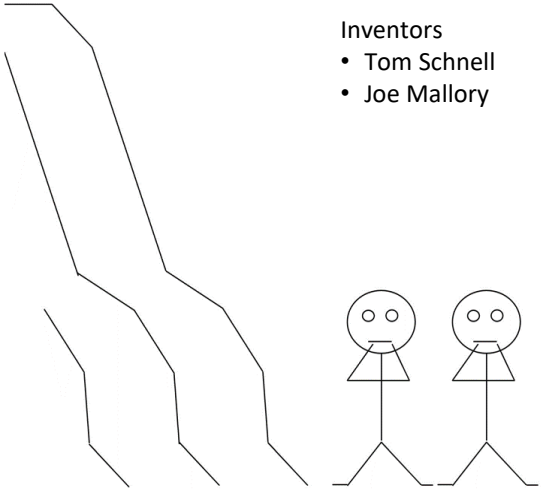
Dell Invention

JEDEC Collaboration



Mobile/Client/AI Computing Forum

The CAMM Journey



Inventors
- Tom Schnell
- Joe Mallory

Step 1: Find Courage, Stamina, Belief, Conviction to climb your mountain

CAMM Invented

2020

Dell CAMM DDR4 System Incubation

2021

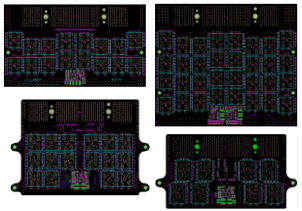
Dell CAMM DDR5 System Dev

2022

Dell Designs all CAMM2 (6 modules)

Dell ships DDR5 CAMM
in Dell Precision 7000 Workstation Notebooks

JEDEC Starts



CAMM2 Builds
DDR5 and LP5 CAMM2
Built by Kingston TECHNOLOGY

2023

Dell Boots CAMM2 Systems (DDR5 and LP5 CAMM2)

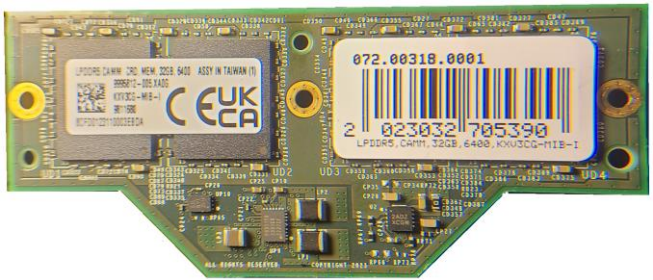
CAMM2 Sponsors
Micron sponsors LP5 CAMM2
Dell sponsors DDR5 CAMM2 (3 designs)
CXMT sponsors DDR5 CAMM2 (1 design)

2024

CAMM = Dell Version
CAMM2 = JEDEC Version

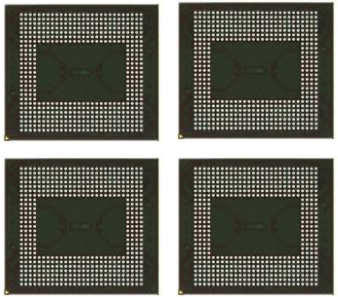
What Problems are solved by LPDDR5 CAMM2?

Compared to LP5 memory down



Dell original LP5 CAMM2, from system incubation Feb'23

- Upgradeability
- Repairability of memory
- MB complexity reduction
- Memory field excursion management
- Lower power relative to SODIMM
- Addresses EU regulations
- Broad support by memory suppliers



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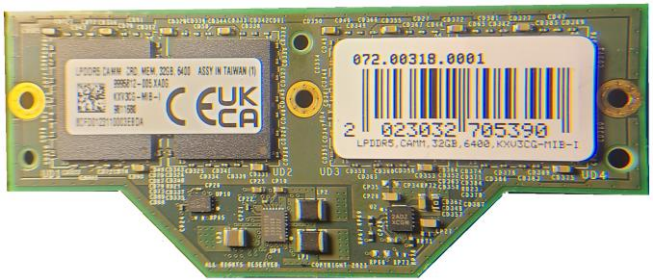

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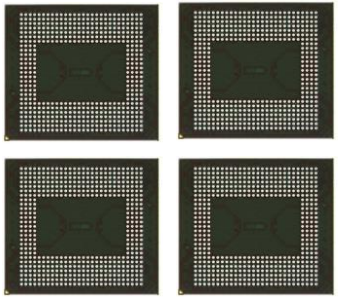


What Problems are created by LPDDR5 CAMM2?

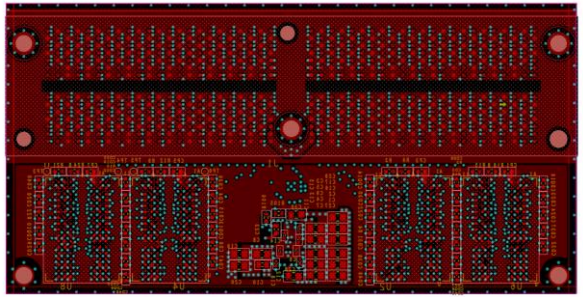
Compared to LP5 memory down

- Total MB area required is higher
- Longer SI channel with connector, relative to memory down, creates a challenge to maintain same bus speed
- Cost relative to memory down will be higher due to added PCB and connector and mechanical parts
- Split VDDQ voltage domain erodes SI margin. The PMIC on module and PMIC on MB supply voltage separate to the DRAM and SOC respectively. Voltage regulator tolerances subtract from overall SI voltage margins

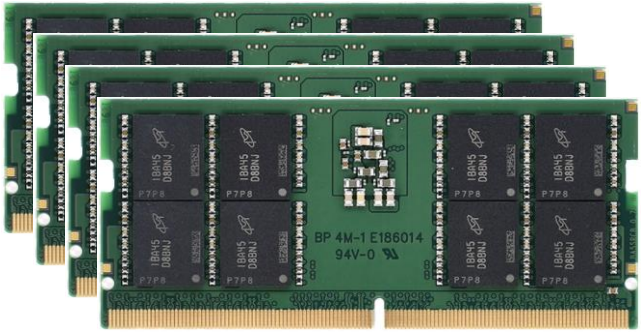
Consensus is strong that problems solved are greatly beneficial over problems created

What Problems are solved by DDR5 CAMM2?

Compared to SODIMM



- Lower total MB area usage
- Improved SI channel
- Reduced length in MB routing
- Tight controls in bus routing
- Scales higher in capacity
- 2DPC problem solved



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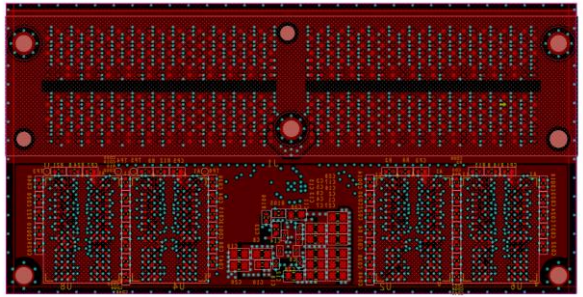

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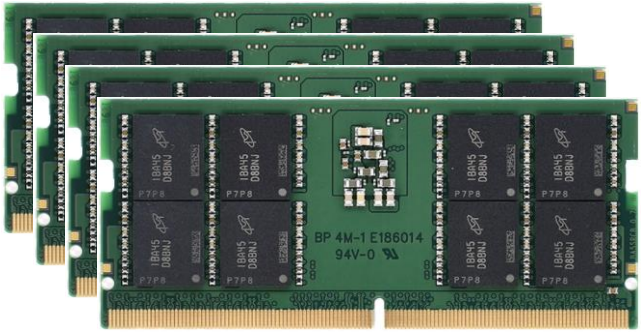


What Problems are created by DDR5 CAMM2?

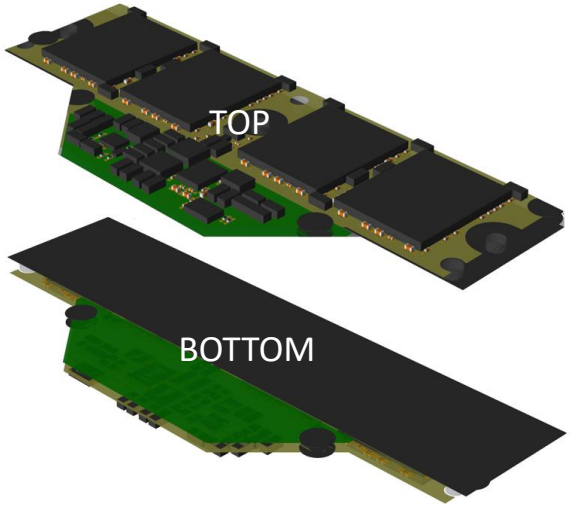
Compared to SODIMM

- Requires tool to install/remove memory module
- CAMM stacking is mechanically complex

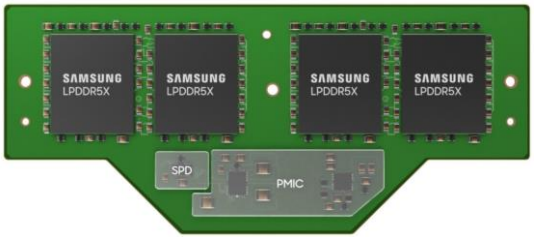
Adoption will slowly ramp until SODIMM is retired, or DDR5 CAMM2's are in market with proven performance advantage

LPDDR5 CAMM2 Variants

DRAM Density	>	Total Capacity
16Gb DRAM	>	16GB, 32GB, 64GB
24Gb DRAM	>	24GB, 48GB, 96GB
32Gb DRAM	>	32GB, 64GB, 128GB



MICRON

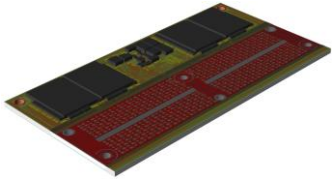


SAMSUNG

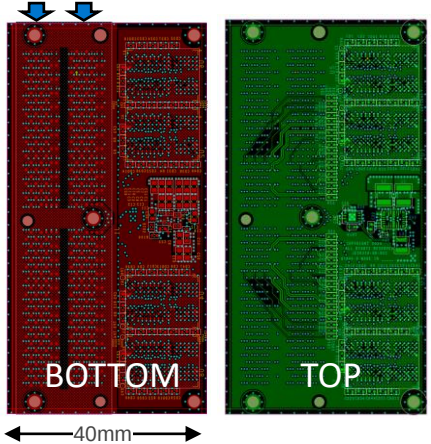
HYNIX

LPDDR5 CAMM2 is growing in popularity and is supported by all Tier1 memory suppliers

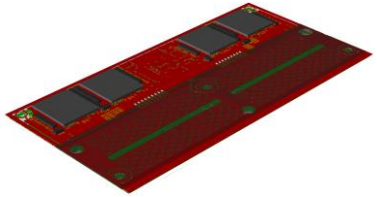
DDR5 CAMM2 Variants



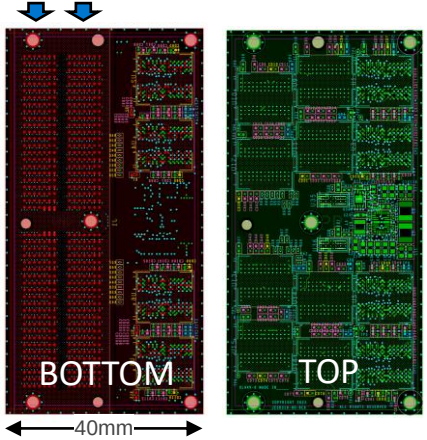
CXXX DC DDR5 CAMM2



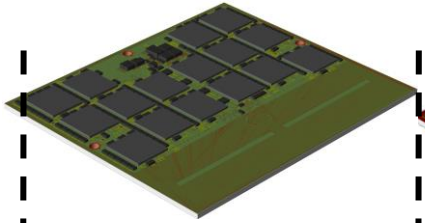
16Gb DRAM > 16GB
24Gb DRAM > 24GB
32Gb DRAM > 32GB
32Gb DDP >



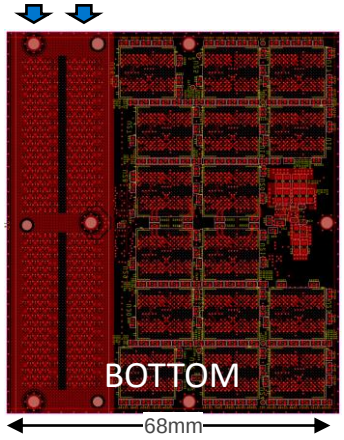
AXXX DC DDR5 CAMM2



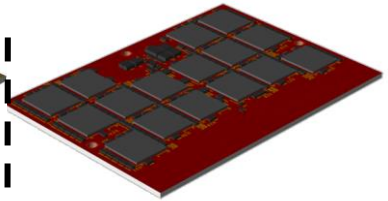
32GB
48GB
64GB
128GB



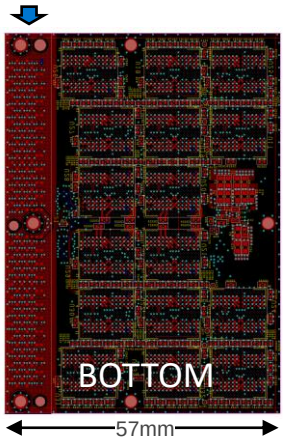
BXXX DC DDR5 CAMM2



64GB
96GB
128GB
256GB



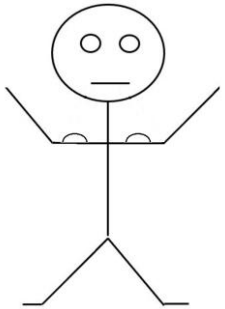
DXXX SC DDR5 CAMM2



64GB (128GB stacked)
96GB (192GB stacked)
128GB (256GB stacked)
256GB (512GB stacked)

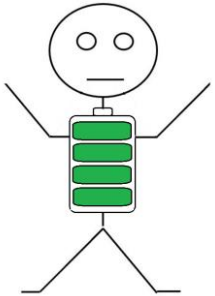
Adoption Dynamics

Memory Industry



DDR5 CAMM2 Claims:

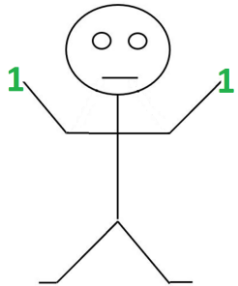
- Higher performance at same bus speed
- Scales to higher capacity
- Alignment with Enterprise
- Cheaper



LPDDR5 CAMM2 Claims:

- Lower power
- Higher bus speed
- Alignment with Mobile
- DRAM not much more $

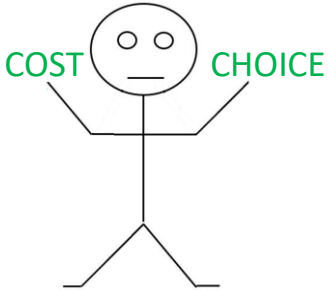
SOC Industry



SOC Desires:

- Pick one. No combo PHYs
- Lower mem power means more power for SOCs
- System cost is not directly under my control

OEM Systems



OEM Desires:

- Lowest cost pressure driven by PC volume
- Choice driven by higher tier segments
- Don't forget desktop/AIO

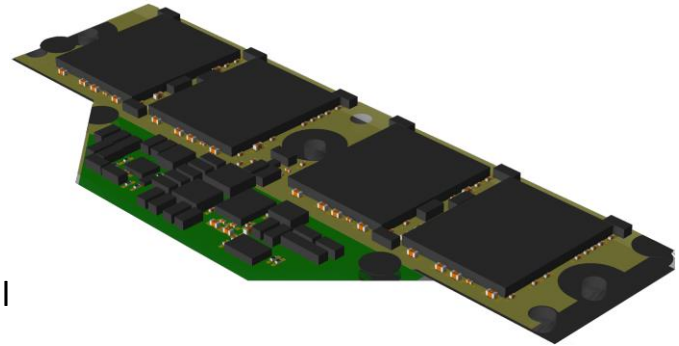
DDR historically higher volume over LPDDR is driven by cost
The debate is settled by SOC roadmaps

CLK
CA[12:0]
DQ[63:32]

Future Work: LPDDR6 CAMM2

LPDDR5 CAMM2 Features:

- Organization
  - 16b / subchannel
  - 32b / channel
  - 128b / module
- Connector Array
  - 14 rows x 46 columns
- VDDQ Split Rail or Common Rail
- Supports Type 3 or 4 MB
- Max Bus Speed = 9.2 GTs



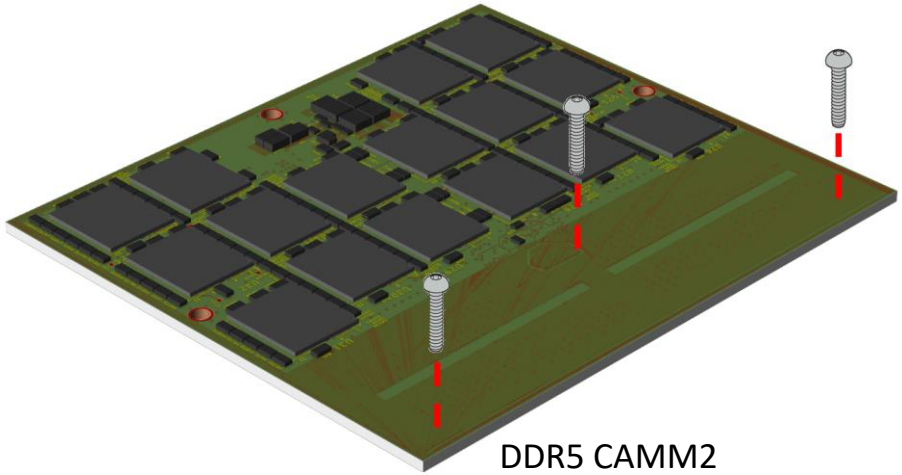
LPDDR6 CAMM2 Features:

- Organization
  - 24b / subchannel
  - 48b / channel
  - 192b /module
- Connector Array
  - ~20 rows x 46 columns
- VDDQ Common Rail
- May support Type 4 PCB only
- Max Bus Speed = ~14.4 GTs

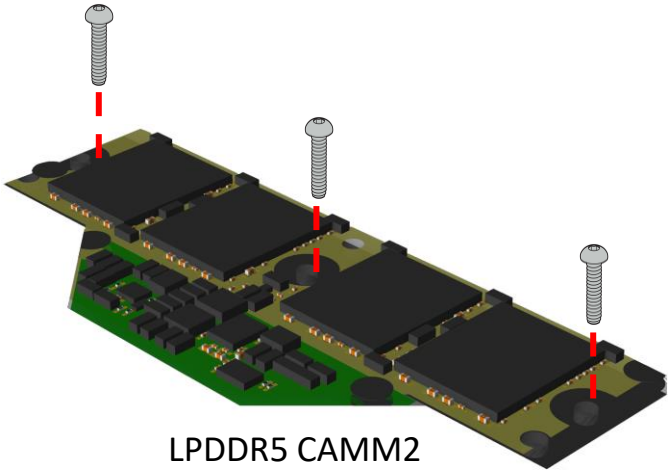
CAMM2 enables max performance or max capacity within the same system

CLK
CA[12:0]
DQ[63:32]

Future Work: Elimination of Screws



DDR5 CAMM2



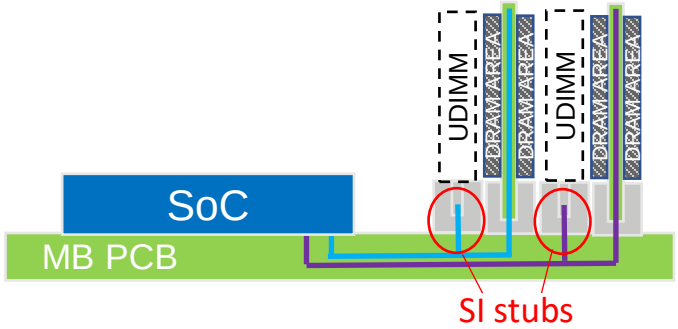
LPDDR5 CAMM2

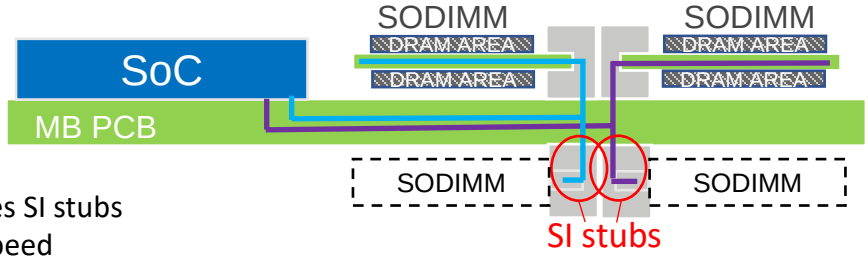
- Need new method to achieve compression without PCB warpage
- Must be toolless
- Must scale to all form factors

Screws have to go!

CLK
CA[12:0]
DQ[63:32]

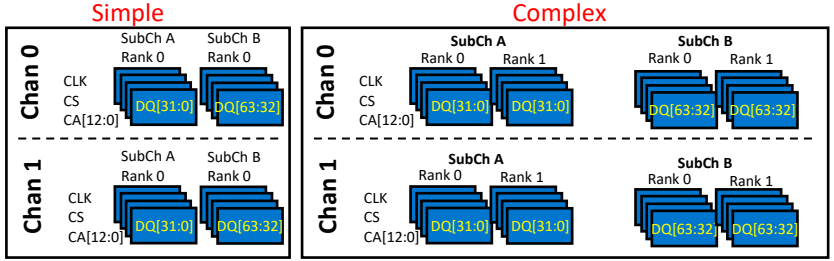
Future Work: The 2DPC Desktop/Server Problem





Mere presence of a soldered connector creates SI stubs which reduces the system capability for bus speed

CAMM2 solves this by moving the topology entirely onto the module
Complexity is handled on the module



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